AN12094

Power Consumption and Measurement of i.MX RT1050

Rev. 1 — 07/2020 Application Note

Contents

1 Introduction

This document discusses about the power consumption of i.MX RT1050, including the following contents:

- i.MX RT1050 overview
- Run mode definition and configuration
- Low-power mode definition and configuration
- How to measure power consumption based on MIMXRT1050 EVK board
- Power consumption under different power modes

The development environment in this application note is IAR Embedded Workbench. Software is based on SDK 2.7.0. The hardware environment is MIMXRT1050 EVKB board (Rev A1).

2 i.MX RT chip overview

The i.MX RT chip is a Cortex-M7 based chip that operates at speed up to 600 MHz to provide high CPU performance and best real-time response.

- Cortex-M7 based processor, which can operate at speed up to 600 MHz.
- Up to 512 KB configurable as Tightly Coupled Memory (TCM).
- Advanced power management module with DCDC and LDO to reduce complexity of external power supply and simplifies power sequencing.
- Various memory interfaces, including SDRAM, Raw NAND FLASH, NOR flash, SD/eMMC, Quad SPI.
- A wide range of other interfaces for connecting peripherals, such as WLAN, Bluetooth™, GPS, displays, and camera sensors.
- Rich audio & video features, including LCD display, basic 2D graphics, camera interface, S/PDIF, and I^2S audio interface.
- Provide rich peripheral modules, such as SPI, I2C, Can, Ethernet, Flex-Timers, and ADC.
- Target at Industrial HMI, Motor Control, and Home Appliance areas.

3 Low power overview

- Power supply
- Run mode
- Low-power mode

3.1 Power supply

Table 1 describes the power supply rails of i.MX RT1050.

Table 1. External power supply rails

Power rail	Description
DCDC_IN	Power for DCDC.
SOC_IN	Power for SOC.
VDD_HIGH_IN	Power for Analog.
VDD_SNVS_IN	Power for SNVS and RTC.
USB_OTG1_VBUS USB_OTG2_VBUS	Power for USB VBUS.
VDDA_ADC_3P3	Power for 12-bit ADC.
NVCC_SD0	Power for GPIO in SDIO1 bank (3.3 V mode).
	Power for GPIO in SDIO1 bank (1.8 V mode).
NVCC_SD1	Power for GPIO in SDIO2 bank (3.3 V mode).
	Power for GPIO in SDIO2 bank (1.8 V mode).
NVCC_GPIO	IO Power for GPIO in GPIO bank.
NVCC_EMC	IO Power for GPIO in EMC bank. (3.3 V mode)
	IO Power for GPIO in EMC bank. (1.8 V mode)

3.2 Run mode

- Run mode definition
- Run mode configurations

3.2.1 Run mode definition

Table 2. Run mode definition

Run mode	Definition
Overdrive run	• CPU runs at 600 MHz, overdrive voltage to 1.275 V • Bus frequency at 150 MHz • All the peripheral is enabled and runs at target frequency • All PLLs are enabled
Full-speed run	• CPU runs at 528 MHz, full loading, lower voltage to 1.15 V • Bus frequency at 132 MHz • All the peripheral is enabled and runs at target frequency • All PLLs are enabled

Table continues on the next page...

Table 2. Run mode definition (continued)

Run mode	Definition
Low-speed run	• CPU runs at 132 MHz, lower voltage to 1.15 V • Internal bus frequency at 33 MHz • All PLL and PFDs are disabled except SYSPLL and SYSPLLPFD2 • 20 % peripheral are active, others are in low-power mode
Low-power run	• CPU runs at 24 MHz, lower voltage to 0.95 V • Internal bus frequency at 12 MHz • All PLLs are powered down, OSC24M powered down, RCOSC24 enabled • High-speed peripherals are power down

3.2.2 Run mode configurations

Table 3. Run mode configurations

	Overdrive run	Full-speed run	Low-speed run	Low-power run
CCM LPM mode	RUN	RUN	RUN	RUN
CPU Core	600 MHz	528 MHz	132 MHz	24 MHz
L1 Cache	ON	ON	ON	ON
IPG CLK	150 MHz	132 MHz	33 MHz	12 MHz
PER CLK	75 MHz	66 MHz	33 MHz	12 MHz
FlexRAM	ON	ON	ON	ON
SOC Voltage	1.275 V	1.15 V	1.15 V	0.95 V
Analog LDO	ON	ON	ON	In Weak Mode
24 MHz XTAL OSC	ON	ON	ON	OFF
24 MHz RC OSC	OFF	OFF	OFF	ON
ARM PLL	ON	ON	Power Down	Power Down
SYS PLL	ON	ON	ON	Power Down
SYS PFD0	ON	ON	Power Down	Power Down
SYS PFD1	ON	ON	Power Down	Power Down
SYS PFD2	ON	ON	ON	Power Down
SYS PFD3	ON	ON	Power Down	Power Down

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Table 3. Run mode configurations (continued)

	Overdrive run	Full-speed run	Low-speed run	Low-power run
USB1 PLL	ON	ON	Power Down	Power Down
USB1 PFD0	ON	ON	Power Down	Power Down
USB1 PFD1	ON	ON	Power Down	Power Down
USB1 PFD2	ON	ON	Power Down	Power Down
USB1 PFD3	ON	ON	Power Down	Power Down
USB2 PLL	ON	ON	Power Down	Power Down
Audio PLL	ON	ON	Power Down	Power Down
Video PLL	ON	ON	Power Down	Power Down
ENET PLL	ON	ON	Power Down	Power Down
Module Clock	ON	ON	On as needed	Peripheral clock off
RTC32K	ON	ON	ON	ON

3.3 Low-power mode

- Low-power mode definition
- Low-power mode configurations
- Wake-up source

3.3.1 Low-power mode definition

Table 4. Low-power mode definition

Low-power mode	Definition
System Idle	• CPU can automatically enter this mode when no thread running • All the peripherals can remain active • CPU only enters WFI mode, it has its state retained so the interrupt response can be very short
Low-power idle	• Much lower power than System Idle mode, with longer exit time • All PLLs are shut off, analog modules running in low-power mode • All high-speed peripherals are power gated, low speed peripherals can remain running at low frequency
Suspend	• The most power-saving mode with longest exit time • All PLLs are shut off, XTAL are off, all clocks are shut off except 32 K clock • All high-speed peripherals are power gated, low speed peripherals are clock gated

Table continues on the next page...

Table 4. Low-power mode definition (continued)

Low-power mode	Definition
SNVS	• All SOC digital logic, analog modules are shut off only except SNVS domain • 32 KHz RTC is alive • VDD_HIGH_IN and VDD_DCDC_IN can be powered off

3.3.2 Low-power mode configurations

Table 5. Low-power mode configurations

	System idle	Low-power idle	Suspend	SNVS
CCM LPM mode	WAIT	WAIT	STOP	—
Arm Core (PDM7)	WFI	WFI	Power Down	OFF
L1 Cache	ON	ON	Power Down	OFF
FlexRAM (PDRET)	ON	ON	ON	OFF
FlexRAM (PDRAM0)	ON	ON	Power down	OFF
FlexRAM (PDRAM1)	ON/OFF	ON/OFF	Power down	OFF
VDD_SOC_IN voltage	1.15 V	0.95 V	0.925 V	OFF
ARM PLL	Power down	Power down	Power down	OFF
SYS PLL	ON	Power down	Power down	OFF
SYS PFD0	Power down	Power down	Power down	OFF
SYS PFD1	Power down	Power down	Power down	OFF
SYS PFD2	ON	Power down	Power down	OFF
SYS PFD3	Power down	Power down	Power down	OFF
USB1 PLL	Power down	Power down	Power down	OFF
USB1 PFD0	Power down	Power down	Power down	OFF
USB1 PFD1	Power down	Power down	Power down	OFF
USB1 PFD2	Power down	Power down	Power down	OFF
USB1 PFD3	Power down	Power down	Power down	OFF
USB2 PLL	Power down	Power down	Power down	OFF
Audio PLL	Power down	Power down	Power down	OFF

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Table 5. Low-power mode configurations (continued)

	System idle	Low-power idle	Suspend	SNVS
Video PLL	Power down	Power down	Power down	OFF
ENET PLL	Power down	Power down	Power down	OFF
24 MHz XTAL OSC	ON	OFF	OFF	OFF
24 MHz RC OSC	OFF	ON	OFF	OFF
LDO2P5	ON	OFF	OFF	OFF
LDO1P1	ON	OFF	OFF	OFF
WEAK2P5	OFF	ON	OFF	OFF
WEAK1P1	OFF	ON	OFF	OFF
Bandgap	ON	OFF	OFF	OFF
Low-Power bandgap	ON	ON	ON	OFF
AHB clock	33 MHz	12 MHz	OFF	OFF
IPG clock	33 MHz	12 MHz	OFF	OFF
PER clock	33 MHz	12 MHz	OFF	OFF
Module clocks	ON as needed	ON as needed	OFF	OFF
RTC32K	ON	ON	ON	ON

3.3.3 Wake-up source

Table 6. Wake-up source

	System idle	Low power idle	Suspend	SNVS
GPIO wake-up	YES	YES	YES	YES (1 PIN only)
RTC wake-up	YES	YES	YES	YES
USB remote wake-up	YES	YES	YES	NO
Other peripheral wake-up sources	YES	YES	YES	NO

NOTE

Irrespective of whether the system is in System Idle, Low-Power Idle or Suspend modes, the wake-up interrupt should be enabled in GPC module. The only pin that can wake up the system in SNVS is IOMUXC_SNVS_WAKEUP_GPIO5_IO00.

Peripheral wake-up requires that the clock for the peripheral is available in the mode.

4 How to measure power consumption on IMXRT1050 EVKB

4.1 IMXRT1050 EVKB (REV A1) board overview

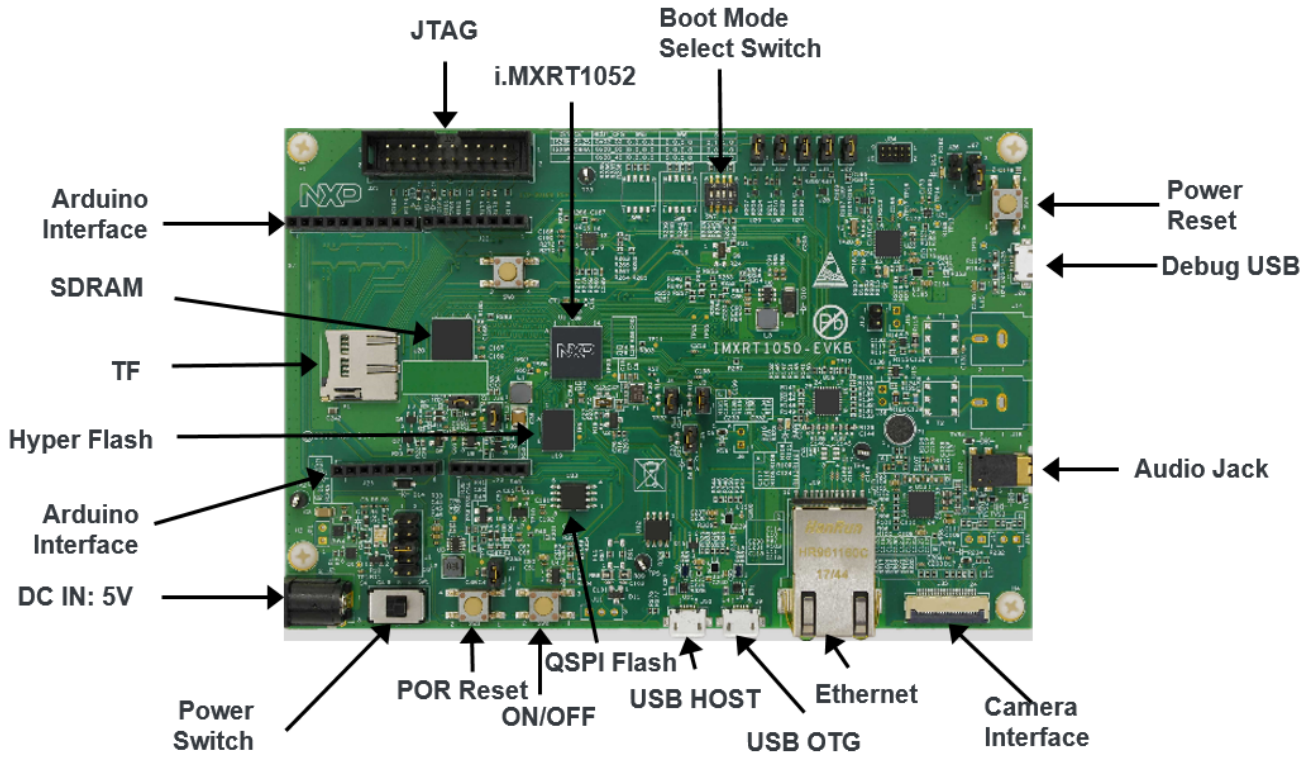

Figure 1. Overview of the IMXRT1050-EVKB board (Front side)

4.1.1 Current measurements on EVK

For this application note, measure the current value of `DCDC_IN` (J37), `VDD_HIGH_IN` (J4), and `VDD_SNVS_IN` (J5).

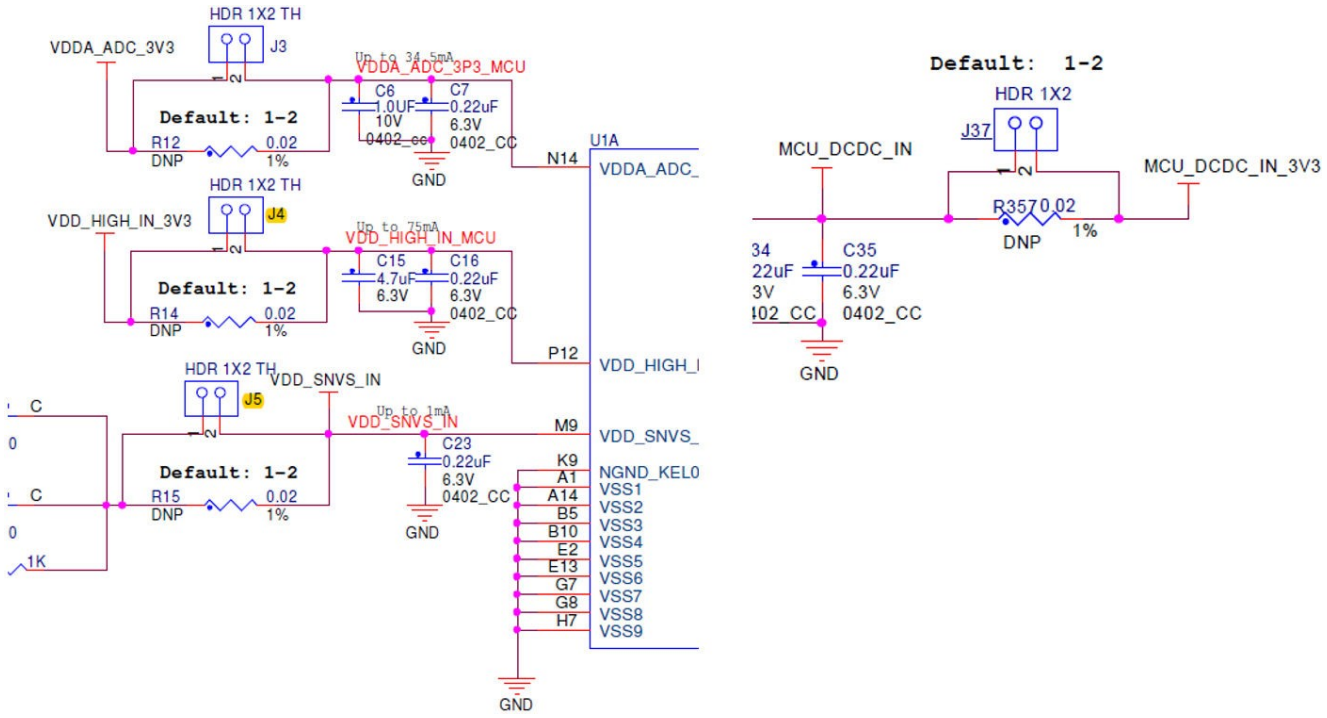

Figure 2. Test points for DCDC_IN, VDD_HIGH_IN and VDD_SNVS_IN

4.1.2 Hardware rework for the EVK

Because the POR_B pin has an internal pullup, R186 and R20 should be removed. Leaving these resistors populated causes higher SNVS current than what is shown in this application note.

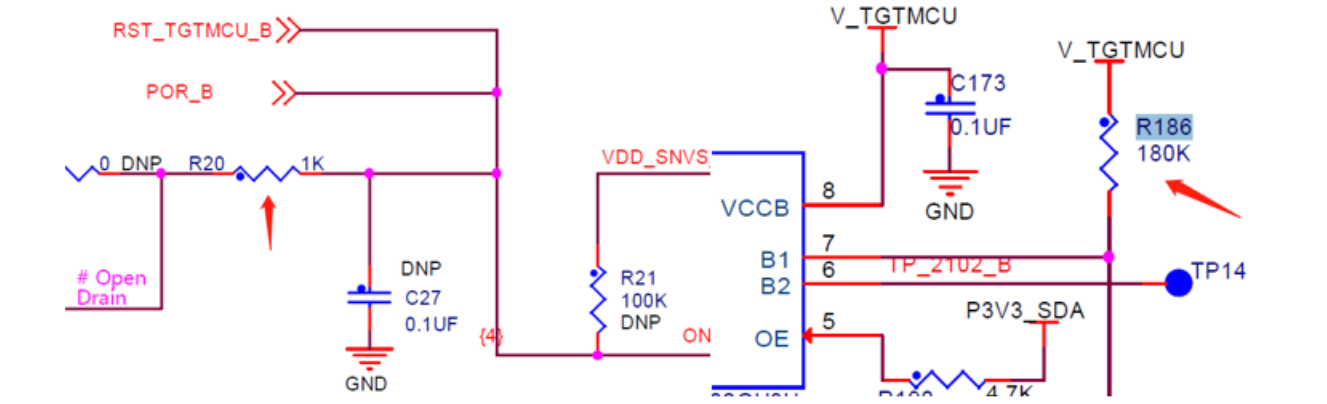

Figure 3. Remove resistors R20 and R186

SNVS_PMIC_STBY_REQ_GPIO5_IO02 outputs a high-level signal under Suspend Mode (Stop Mode). On the EVK board, this pin is used to control LCD Power switch and a resistor R31 is connected to this pin. When the chip is under the Suspend Mode, this resistor consumes more current. To fix this issue, SNVS_PMIC_STBY_REQ is configured as a low-level output GPIO pin.

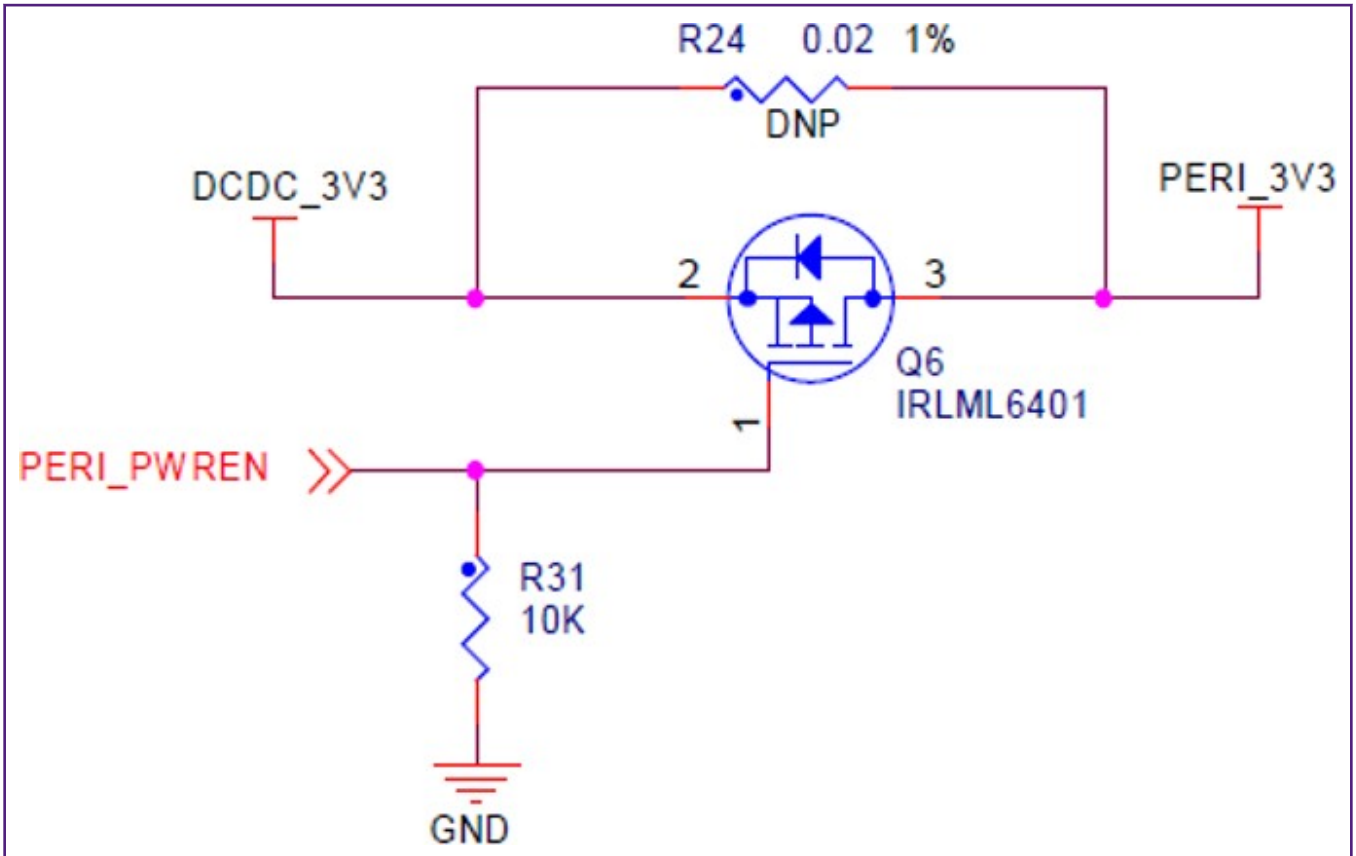

Figure 4. LCD 3V3 power switch circuit

4.1.3 Run IAR-based project demo example - Power mode switch

- The project file is located at:

```
SDK_2.7.0_EVKB-IMXRT1050\boards\evkbimxrt1050\demo_apps\power_mode_switch_bm\iar
```

- Download the project.
- Select the target power mode on the terminal.

5 Power consumption results

NOTE

To reduce power consumption, `VDD_SNVS_IN` is powered by `VDD_HIGH_IN` in all power modes except the SNVS mode.

All power consumption values are typical silicon at 25 C.

Discontinuous Conduction Mode (DCM) increases the efficiency of DCDC in case of low current loading and is always recommended.

5.1 RUN mode

The power consumption in Table 7 and Table 8 is measured with the default SDK low-power mode switch project.

Table 7. RUN mode on RAM (While 1)

RT1050-EVK		Overdrive (600 MHz)		Full-speed run (528 MHz)		Low-speed run (132 MHz)		Low-power run (24 MHz)	
Power rail	Voltage (V)	Current (mA)	Power (mW)	Current (mA)	Power (mW)	Current (mA)	Power (mW)	Current (mA)	Power (mW)
DCDC_IN	3.3	40.135	132.4455	29.92	98.736	10.95	36.135	2.03	6.699
VDD_HIGH_IN	3.3	20.47	67.551	20.395	67.3035	4.6	15.18	0.304	1.0032
VDD_SNVS_IN	3.3	0.0105	0.03465	0.00895	0.029535	0.00195	0.006435	0.00515	0.016995

Table 8. RUN mode XIP on Flash (While 1)

RT1050-EVK		Overdrive (600 MHz)		Full-speed run (528 MHz)		Low-speed run (132 MHz)		Low-power run (24 MHz)	
Power rail	Voltage (V)	Current (mA)	Power (mW)	Current (mA)	Power (mW)	Current (mA)	Power (mW)	Current (mA)	Power (mW)
DCDC_IN	3.3	34.885	115.1205	26.61	87.813	10.95	36.135	1.785	5.8905
VDD_HIGH_IN	3.3	20.425	67.4025	20.47	67.551	4.59	15.147	0.2965	0.97845
VDD_SNVS_IN	3.3	0.0104	0.03432	0.0089	0.02937	0.0019	0.00627	0.00515	0.016995

The power consumption in Table 9 and Table 10 is measured with the CoreMark which based on low-power mode switch project.

Table 9. CoreMark on RAM

RT1050-EVK		Overdrive (600 MHz)		Full-speed run (528 MHz)		Low-speed run (132 MHz)		Low-power run (24 MHz)	
Power rail	Voltage (V)	Current (mA)	Power (mW)	Current (mA)	Power (mW)	Current (mA)	Power (mW)	Current (mA)	Power (mW)
DCDC_ IN	3.3	68.67	226.611	50.05	165.165	15.705	51.8265	2.755	9.0915
VDD_H IGH_IN	3.3	20.51	67.683	20.37	67.221	4.55	15.015	0.305	1.0065
VDD_S NVS_IN	3.3	0.01105	0.036465	0.00925	0.030525	0.0021	0.00693	0.00525	0.017325

Table 10. CoreMark XIP on Flash

RT1050-EVK		Overdrive (600 MHz)		Full-speed run (528 MHz)		Low-speed run (132 MHz)		Low-power run (24 MHz)	
Power rail	Voltage (V)	Current (mA)	Power (mW)	Current (mA)	Power (mW)	Current (mA)	Power (mW)	Current (mA)	Power (mW)
DCDC_IN	3.3	62.65	206.745	43.98	145.134	15.54	51.282	2.45	8.085

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Table 10. CoreMark XIP on Flash (continued)

RT1050-EVK		Overdrive (600 MHz)		Full-speed run (528 MHz)		Low-speed run (132 MHz)		Low-power run (24 MHz)	
Power rail	Voltage (V)	Current (mA)	Power (mW)	Current (mA)	Power (mW)	Current (mA)	Power (mW)	Current (mA)	Power (mW)
VDD_HIGH_IN	3.3	20.4	67.32	20.36	67.188	4.65	15.345	0.2965	0.97845
VDD_SNVS_IN	3.3	0.01115	0.036795	0.00935	0.030855	0.002	0.0066	0.00525	0.017325

5.2 Low-power mode

The power consumption in Table 11 and Table 12 is measured with the power mode switch project.

Table 11. Power consumption results

RT1050-EVK	System Wait mode			Low-power Idle mode			Suspend mode			Shutdown the system		
Power rail	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)
DCDC_IN	3.3	4.13	13.629	3.3	0.885	2.9205	3.3	0.9	2.97	0	0	0
VDD_HIGH_IN	3.3	4.675	15.4275	3.3	0.3	0.99	3.3	0.036	0.1188	0	0	0
VDD_SNVS_IN	3.3	0.05735	0.189255	3.3	0.00515	0.016995	3.3	0.00045	0.001485	3.3	0.014	0.0462

Table 12. Low power mode XIP on Flash

RT1050-EVK	System Wait mode			Low-power Idle mode			Suspend mode			Shutdown the system		
Power rail	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)
DCDC_IN	3.3	5.67	18.711	3.3	0.985	3.2505	3.3	0.115	0.3795	0	0	0
VDD_HIGH_IN	3.3	4.57	15.081	3.3	0.2915	0.96195	3.3	0.0355	0.11715	0	0	0
VDD_SNVS_IN	3.3	0.0015	0.00495	3.3	0.00505	0.016665	3.3	0.00045	0.001485	3.3	0.014	0.0462

NOTE

All power consumption values are typical silicon at 25 C.

Discontinuous Conduction Mode (DCM) increases the efficiency of DCDC in case of low current loading and is always recommended.

To reduce power consumption, VDD_SNVS_IN is powered by VDD_HIGH_IN in all power modes except the SNVS mode.

6 Conclusion

This document mainly describes how to measure power consumption on i.MX RT based on IMXRT1050 EVKB (Rev. A1). For more design details in designing a low-power application, see *How to use i.MX RT Low Power Feature* (document AN12085).

7 Revision history

Table 13. Revision history

Revision number	Date	Substantive changes
0	09/2018	Initial release
1	07/2020	Replace A0 silicon data with B0 silicon's data

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