NXP Semiconductors
Application Note

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i.MXRT1050 Migration Guide

Migrating from silicon Rev A0 to Rev A1

Contents

1. Introduction

1.1. Purpose

This Application Note is a migration guide for i.MXRT1050 users that are migrating from silicon Rev. A0 to Rev. A1.

1.2. Scope

This document provides differentiation from hardware

and software scope. For details on A0, A1 part number and decoder, refer to Table 1.

For all users, suggest to use A1 silicon for own board design.

For those who are evaluating i.MXRT1050 with EVKA board, please refer to the summary table for SW and HW changes.

For those who will evaluate i.MXRT1050 with EVKB board, suggest to use latest SDK with workaround listed in summary table.

Table 1. A0, A1 part number and decoder

Part number	Rev A0	Rev A1
	MIMXRT1052CVL5A	MIMXRT1052CVL5B
	MIMXRT1052DVL6A	MIMXRT1052DVL6B
	MIMXRT1051CVL5A	MIMXRT1051CVL5B
	MIMXRT1051DVL6A	MIMXRT1051DVL6B
Board name	MIMXRT1050-EVK	IMXRT1050-EVKB

1.3. Reference

For RT1050 reference manual, datasheet and all support docs please refer to below link:
https://www.nxp.com/imxrt1050

2. Summary

Table 2. Summary table

Category	Items	Silicon change from A0 to A1	HW Change	SW Change
Power	ERR011091 bug fix	IO: fix the issue that high POR current if NVCC_GPIO/EMC is powered ahead of VDD_SOC_IN	For silicon A0: 1. DCDC_IN need powered together or ahead of SNVS power domain. 2. DCDC_IN need to be at 2.8V~3.0V. 3. DCDC_PSWITCH not working. For silicon A1, recommend customer to modify HW board as below: 1. DCDC_IN powered together with another IO domain (IMXRT1050-EVKB: DNP R42, populate R25).	No
	ERR011092 bug fix	DCDC: fix the issue that normal power up sequence may result in DCDC startup failure		No

Category	Items	Silicon change from A0 to A1	HW Change	SW Change
	ERR011093 bug fix	DCDC: Fix the issue that unexpected DCDC reset occurs on some chips	2. SNVS power support options: 1)SNVS power ahead of other power domains by dedicated LDO(IMXRT1050-EVKB: populate R34,DNP R354 by default). 2)SNVS power together with other power domain if SNVS mode is not necessary(IMXRT1050-EVKB: DNP R34,R38 and U5,populate R354 and R35). 3.DCDC_PSWITCH should be 1ms behind DCDC_IN(IMXRT1050-EVKB: change R32 from 0 to 30Kohm). 4.DCDC_IN change to 3.3V instead of 3.0V(IMXRT1050-EVKB: change R305 from 402K to 464K).	No
Interface	GPIO new feature	Giada bit wise set/clear/toggle function	No	Release GPIO bit set/clear/toggle API
	ERR011138 bug fix	LCDIF: LUT consecutive programming may fail in case two writes are close	No	Remove software workaround in SDK
Memory	Cache improvement	SOC:OCRAM, FlexSPI, SEMC can't response CM7 cache speculative read when their clock is turned off	No	For A1 silicon, customer must keep below register field: SEMC:CCM_CCGR1 CG9(semc_exsc clock) need to be 2'b11 as default from reset FLEXSPI:CCM_CCGR0 CG3(flexspi_exsc clock) need to be 2'b11 as default from reset OCRAM:CCM_CCGR2 CG0(ocram_exsc clock) need to be 2'b11 as default from reset
	SEMC	CCM: add bit filed to control semc_exsc clock, must be enabled always	No	
	FLEXSPI	CCM: add bit filed to control flexspi_exsc clock, must be enabled always	No	
	OCRAM	CCM: add bit filed to control ocram_exsc clock, must be enabled always	No	

Category	Items	Silicon change from A0 to A1	HW Change	SW Change
Others	Chip ID	Changed from 1.0 to 1.1	No	Since the silicon revision is updated, user software will have to accommodate this change if this silicon revision is used
	ERR011164 bug fix	ADC: ADC_ETC fails to clear the ADC_ETC request signals automatically after receiving DMA ack	No	No
	ERR011111 bug fix	Chip stuck in reset when RTWOG low byte test mode is enabled	No	No
	ERR011165 bug fix	SNVS: Invalid ECC check failure	No	No
	ERR011110 bug fix	System Boot: SEMC NOR boot cannot support the signed image authentication under HAB closed mode	No	No
	ERR011119 bug fix	System Boot: FlexSPI NOR encrypted XIP boot fails after system reset if the FAC region number is less than 2	No	No
	ERR011120 bug fix	System Boot: FlexSPI NOR encrypted XIP boot fails after system reset if the IOMUXC_GPR18 to IOMUXC_GPR21 are locked	No	No
	ERR011150 bug fix	Internal BCLK is not generated if it is disabled when DIV > 0 and then enabled again	No	No
	DCDC Trim	ROM: add DCDC trim function in ROM code	No	No
	OTPMK Selection	SOC: blown the OTP_KEY_TO_DCP_DISABLE fuse bit to protect to OTPMK key	No	For A1 part, customer has to keep HAB close when encrypt XIP image by selecting OPTMK as key
	SOC	CCM：add bit field for mainclk clock gate	No	For A1 silicon, keep the below register field: CCM_CCGR0：CG4（sim_m or sim_main register access clock）need to be 2'b11 as default from reset

Category	Items	Silicon change from A0 to A1	HW Change	SW Change
				CCM_CCGR4：CG0（sim_m7 register access clock）need to be 2'b11 as default from reset

3. Revision history

Table 3. Revision history

Revision number	Date	Substantive changes
0	03/2018	Initial release
1	05/2018	Updated Table 2. Summary table for DCDC Trim, OTPMK Selection, and SOC.

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